METHOD FOR REDUCING SINGLE BIT DATA LOSS IN A MEMORY CIRCUIT Filing Date: August 25, 1999

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(Amended) The method of claim 7 and further comprising forming a film comprising 9. Hydrogen isotope within the gate region of the memory circuit in order to reduce single bit data loss.

(Amended) A method of forming a non-volatile electrically alterable semiconductor 26. memory cell with reduced, random, single bit data loss in a memory circuit comprising:

providing a silicon substrate;

fabricating a field oxide region and a channel region over or within the silicon substrate; growing an oxide over the channel region in an atmosphere

enriched in Hydrogen isotope;

fabricating at least one gate member; and

passivating the memory cell comprising single bit data in an atmosphere that comprises

Hydrogen isotope thereby reducing single bit data loss.

(Amended) A method for passivating a non-volatile, electrically alterable semiconductor 35. memory cell, thereby reducing random, single bit data loss in a memory circuit, comprising: providing a non-volatile, electrically alterable semiconductor memory cell comprising single bit data; and exposing the memory cell to/an atmosphere that comprises Hydrogen isotope thereby reducing single bit data loss.

(Amended) A method for overlaying source and drain regions of a non-volatile, 37. electrically alterable semiconductor memory cell with a thermal oxide layer thereby reducing random, single bit data loss in a memory circuit, comprising:

providing a silicon substrate and providing a memory cell comprising single bit data; defining source and drain regions in the silicon substrate; and growing the thermal oxide layer over the source and drain regions in an atmosphere that comprises Hydrogen isotope thereby reducing single bit data loss

in the memory cell.